AMENDMENT(S) TO THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 19, with the following rewritten paragraph:

In the related memory system, the motherboard transmission bus lines are equal to the connectors in number. Accordingly, the memory system has a disadvantage that the transmission bus lines have a long total length and a complicated arrangement. Thus, this type of the memory system is ~~hard~~ difficult to ~~be designed~~ design in a case where it has more connectors.

Please replace the paragraph beginning at page 2, line 17, with the following rewritten paragraph:

According to a first aspect of this invention, a memory module ~~is possible to~~ can be inserted in any one of connectors formed on a motherboard. The memory module comprises a memory chip. A pin is connectable to the connector. A bus connects the memory chip to the pin. A terminating resistor is connected to one end of the bus. A stab resistor is connected between the pin and the other end of the bus.

Please replace the paragraph beginning at page 5, line 10, with the following rewritten paragraph:

The memory board 11 is a printed circuit board. The memory chips 12 are mounted on the memory board 11 and arranged at regular intervals. The module transmission bus line 13 is formed on the memory board 11 to connect the memory chips [[11]] 12 to specific one of the pins 14 in common. That is, the specific pin is connected to an end of the module transmission bus line 13. The pins 14 [[is]] are connectable to terminals of a connector mounted on a motherboard. The terminating resistor 15 is connected to the other end of the module transmission bus line 13 at one end thereof and supplied with a predetermined voltage level of Vterm at the other end thereof.

Please replace the paragraph beginning at page 6, line 4, with the following rewritten paragraph:

The structure of Fig. 2 needs the same number of the motherboard transmission bus lines 23 as the connectors 22. This is because the connectors 22 are individually connected to the memory controller 21 with the motherboard transmission bus lines 23 as mentioned above. Accordingly, the total length of the motherboard transmission bus lines 23 becomes large in roughly proportion to the number of the connectors 22. Furthermore, it becomes difficult to ~~arrangement of~~ arrange the motherboard transmission bus limes 23 with increase of the total length thereof. Thus, it is hard to design a memory system having more connectors (and memory modules).

Please replace the paragraph beginning at page 7, line 5, with the following rewritten paragraph:

Referring to Fig. 3, ~~the~~ a description ~~will be made~~ follows about a preventive method for preventing a reflected signal from being caused [[on]] in a star connection to foster better understanding of this invention.

Please replace the paragraph beginning at page 8, line 3, with the following rewritten paragraph:

Additionally, Japanese Unexamined Patent Publication No. 2001-84070 discloses a method for finding resistance of two stab resistors (N=2) in a transmission line having two branches. However, the method is not applicable to a case where the number of branches is equal to or more than three (N?3). Furthermore, the method is for a liquid crystal display panel and the publication does not suggest that it is applicable to a memory system, especially a high speed memory system. The method is on condition that termination resistors are not connected to ends of the wires and that reflection occurs at the ends of the wires. Furthermore, the method is impossible to be applied to the memory system because it fixes a characteristic impedance of one of the wires at first and then ~~decide characteristics impedance~~ decides characteristic impedances of the remaining two wires and resistors.

Please replace the paragraph beginning at page 8, line 23, with the following rewritten paragraph:

In the application, it is undesirable that stab resistors ~~are~~ be provided on a motherboard. This is because the manufacturer of the motherboard generally prohibits alterations of the motherboard. That is, if the stab resistors are formed on the motherboard, it is impossible to exchange them for other resistors. There is a variety of needs of users ~~about~~ regarding the number of the memory modules. To meet the needs, it is necessary to be able to change resistance of each stab resistor according to the number of the memory modules (or branches).

Please replace the paragraph beginning at page 11, line 29, with the following rewritten paragraph:

In each of the memory systems 60 and 70, the module transmission bus lines 53 or 32 and the motherboard transmission bus line 63 or 73 is used for an IO bus line (or a bi-directional bus). Each of the memory chips 51 comprises a driver and a receiver connected to the IO bus line. Each of the memory controllers 61 and 71 similarly comprises a driver and a receiver connected to the IO bus line. In Fig. 6, two sets of the driver and the receiver are designated by small triangles in the memory controller 61 and one of the memory chips 52. Similarly, Fig. 7 shows other two sets of the driver and the receiver with small triangles.

Please replace the paragraph beginning at page 12, line 11, with the following rewritten paragraph:

The memory module 50 has a memory chip arrangement portion which ~~consist~~ consists of the memory chips 52 and the module transmission bus line 53. The memory chip arrangement portion has effective impedance Zeffdimm (corresponding to the Zdimm of Fig. 4). Here, it is assumed that the module transmission bus line 53 has wiring impedance of Z0 (= $\sqrt{L/C}$) [Ω], an interval between adjacent two memory chips 52 is represented by X [m], and input capacitance is represented by Cin [F]. Then the effective impedance Zeffdimm of the memory chip arrangement portion is given by:

$$Zeffdimm = \sqrt{L/(C + Cin/X)}\,.$$

For instance, the effective impedance Zeffdimm is approximately equal to 39.3[Ω] when Z0=60[Ω] ($L=3.6\times10^{-7}$[H/m], $C=1.0\times10^{-10}$[F/m]), $X=12\times10^{-3}$[m], and $Cin=1.6\times10^{-12}$[F]. Moreover, the effective impedance Zeffdimm is approximately equal to 43.3 [Ω] when Z0 = 60[Ω] ($L=3.6\times10^{-7}$[H/m], $C=1.0\times10^{-10}$[F/m]), $X=13\times10^{-3}$[m], and $Cin=1.2\times10^{-12}$[F].

Please replace the paragraph beginning at page 13, line 24, with the following rewritten paragraph:

The memory systems shown in Figs. 6 and 7 can stably operate faster than an existing memory system called DDR-I (operating frequency: 133 MHz) or DDR-II (operating frequency: 266 MHz). For example, the operating frequency of the memory systems ~~operate~~ is over 300 MHz ~~of the operating frequency~~. This is because no signal reflection occurs at ~~all~~ any of the branch points and end portions.

Please replace the paragraph beginning at page 14, line 1, with the following rewritten paragraph:

Furthermore, each of memory systems of Figs. 6 and 7 does not need a stab resistor on the motherboard. Accordingly, the motherboard has a small number of elements and broad spaces for wiring. In addition, there is no attenuation of transmission signal on the motherboards in the memory systems of Figs 6 and 7. Additionally, the structure of the memory systems of Figs. 6 and 7 allows a ~~multi-slot~~ multi-slot system to be formed without a large increase of wires on the motherboard.

Please replace the paragraph beginning at page 14, line 9, with the following rewritten paragraph:

Though the above description ~~is made about~~ concerns applying this invention to the bi-directional bus as the IO bus of the memory system, this invention is applicable to an unidirectional bus as a command address bus of the memory system as illustrated in Fig. 10 or 11. In such a case, the wiring impedance Zmb of the motherboard, the stab resistance Rs and the

effective impedance Zeffdimm can be found by the use of the equations (6) and (7). However, they may be found by the use of the equation (4).

Please replace the paragraph beginning at page 15, line 1, with the following rewritten paragraph:

Though the terminating resistor 55 is formed at the outside of the memory chips 52 on the memory board 51, the terminating resistor 55A may be formed in the one of memory chips 32A as illustrated in Fig. 12. This is known as a technique called "On Die Termination".

Please replace the paragraph beginning at page 15, line 6, with the following rewritten paragraph:

Next, referring to Figs. 13 to 15, ~~the~~ a description ~~will be made about~~ follows regarding a memory module according to another embodiment of this invention and about memory systems using the memory modules.

Please replace the paragraph beginning at page 15, line 13, with the following rewritten paragraph:

The memory board 131 is a printed circuit board. The memory chips 132 are mounted on the memory board 131 at regular intervals. The module IO bus lines 133 are formed on the memory board 131 to be connected to the memory chips 132, respectively. The terminating resistors 134 are formed in the memory chips 132 and connected to ends of the memory ~~bas~~ bus lines 133, respectively. The stab resistors 135 are formed on the memory board to be connected to other ends of the module IO bus lines 133, respectively. The pins ~~135~~ 136 are formed at the edge [[on]] of the memory board 131. Each of the stab resistors 135 is also connected to a corresponding one of the pins 135.

Please replace the paragraph beginning at page 16, line 1, with the following rewritten paragraph:

The memory controller 141 is formed on the motherboard. The connectors 142 are mounted on the motherboard to receive the memory modules of Fig. 13. The motherboard IO bus lines 143 are formed on the motherboard to be connected to the connectors 142. The motherboard IO bus lines 143 are corresponding to the memory chips ~~133~~ 132 of each memory module 130 respectively. Each of the motherboard IO bus lines 143 connects corresponding memory chips on the memory modules 130 with one another. That is, according to this embodiment, not memory modules but memory chips are connected to one another in a stab connection.

Please replace the paragraph beginning at page 16, line 11, with the following rewritten paragraph:

In this embodiment, bi-directional transmission can be carried out without signal reflection between the memory controller and each memory chip if resistance of the terminating resistors 134 and the stab resistors 135 are found by the use of the equations (6) and (7). However, the effective impedance Zeffdimm depends on the memory chip ~~134~~ 132 and the module IO bus line ~~132~~ 133 connected to the memory chip ~~134~~ 132.